A 40 Gbit/s SUPER-DYNAMIC DECISION IC USING 0.15-μm GaAs MESFETs

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ABSTRACT

This paper describes a 40 Gbit/s decision IC using 0.15-μm gate length GaAs MESFETs. A super-dynamic flip-flop circuit and wideband amplifier were applied in order to attain 40 Gbit/s operation. The IC is the first to provide an error-free 40 Gbit/s decision operation.

INTRODUCTION

Emerging lightwave communications technologies are about to bring 10-Gbit/s systems into commercial use[1]. Because of the growth in multimedia services, larger transmission capacity will be required to back-bone networks. Intensive efforts are underway to develop large capacity systems using WDM and TDM technologies. Recently, 40 Gbit/s based WDM and TDM transmission experiments in the research stage were successfully carried out [2][3]. The role of high-speed and reliable electronic components becomes more important in order to develop cost effective systems. Furthermore, an operation speed of over 40 Gbit/s is required.

In these broadband optical fiber communication systems, a decision circuit is an indispensable component to realizing regeneration functions. In the last few years, various kinds of high-speed decision circuits with HBT [4], HEMT [5], Si bipolar [6] and GaAs MESFET[7] technologies have been reported. The record bit rate of 40 Gbit/s has been reported for a AlGaAs/GaAs HBT IC [4]. However, an error-free operation at this bit-rate has not been confirmed.

This paper describes a 40 Gbit/s decision IC using 0.15-μm gate length GaAs MESFETs. There are two keys to attaining high-speed decision circuit operation. First is the high-speed flip-flop circuit. We adopt the super-dynamic flip-flop circuit [7] because its high speed operation using production-level GaAs MESFETs has been confirmed. The second key is the wideband amplifier. We adopt a parallel feedback amplifier and an inductor peaking amplifier for input and output buffers. By using these circuit technologies, an error-free 40 Gbit/s decision circuit operation is confirmed for the first time.

CIRCUIT DESIGN

A. Super-dynamic Flip-Flop

The super-dynamic D-type flip-flop (FF) circuit [7] is shown in Fig. 1. The circuit features are (1) a series-gate connection to separate the current path of the reading and latching circuits; (2) a smaller latching current (I-latch) than the reading current (I-read); and (3) a source coupled negative feedback pair (SCNFP) inserted in the first-level latching differential pair in a cascode manner.

The schematic output waveform of the super-dynamic D-FF at low frequency is shown in Fig. 2. Due to the negative feedback action of the SCNFP, the input data information is stored only for a short time at every transition between the reading and latching operation. This makes the FF operate dynamically, which means that the FF has a minimum operation bit-rate. The SCNFP can drastically reduce the effective logic swing from R_LI-read to R_L/2(I-read - I-latch) without any degradation of the signal transition slew rate, where R_L is the load resistance. This leads to higher speed operation than conventional FFs.

Figure 3 shows the operation speed of the super-dynamic decision IC versus gate width ratio, Wg-latch/Wg-read, which corresponds to I-latch/I-read. The circuit performance was simulated by HSPICE using the transistor parameters of the 0.15-μm gate-length GaAs MESFETs. The operation speed was simulated under the condition that the output voltage and the phase margin are larger than 700 mVp-p and 180 degrees, respectively. In this case, a repeated (1000) pattern was used for the input data signal. The gate-width ratio and load resistance R_L were fixed to optimized values of 30 μm and 350 Ω, respectively. The maximum operation speed increases as the gate-width ratio increases. The minimum operation

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speed also increases as the gate-width ratio increases. In order to obtain high-speed operation with a wide operation range, we adopted the gate-width ratio of 0.5. The maximum speed at this ratio is 100 % higher than that of the conventional static master-slave FF.

B. Wideband input and output buffers

As the core D-FF speed increases, the bandwidth of conventional clock and data buffers can no longer cover the flip-flop operation range. It has been reported that the bandwidth of the clock buffer causes degradation in the retiming capability of D-FFs [7]. Since the super-dynamic D-FF has a minimum operation clock frequency, its clock buffer does not need a broad-band operation from DC. Therefore, an AC-coupled passive level shifter, which consists of a blocking capacitor and a resistive divider, was adopted for the clock buffer. This results in a significant improvement on the buffer bandwidth.

On the other hand, the data buffer and output buffer require a wide bandwidth from DC to the maximum FF operation frequency, high gain and its gain flatness. These factors affect the input sensitivity of the decision IC and its output waveform quality. These buffers are usually required to cover the bandwidth approximately over 70% of the input data bit-rate. A parallel feedback amplifier [8], shown in Fig. 4, is employed in the data input buffer and an inductor-peaking amplifier, shown in Fig. 5, is adopted for the output buffer. For these buffers, capacitance peaking was also added to the source follower circuits to compensate for the loss of the source follower. Figures 6 and 7 show the simulated gain-bandwidth characteristics of the input and output buffers, respectively. Simulation results indicate that both of the 3 dB down bandwidths of the data input and output buffers are improved by 70% compared to those of conventional buffers. They almost cover the required bandwidth for the 40 Gbit/s data signal.

EXPERIMENTS

A. Decision Circuit Configuration

The block diagram of the super-dynamic decision IC is shown in Fig. 8. The IC consists of input data buffers, a clock buffer, a core D-type flip-flop (D-FF), an output buffer, and an open drain output driver. These components are designed as SCFL (Source Coupled FET Logic) series-gated circuits. The IC has a single data input and a differential output, which are connected to an impedance-matched 50 Ω and a 100 Ω termination resistor, respectively, to obtain clear eye patterns. These inputs and outputs can be directly connected to SCFL interfaces.

B. Device Performance

The IC was fabricated with 0.15 μm self-aligned Au/WSiN-gate GaAs MESFETs [9]. A 0.15 μm gate-length was obtained by i-line photolithography with shrinkage of the resist size by O_2-RIE and ECR-etching. Furthermore, a two-step buried p-layer LDD structure was applied in order to suppress the short channel effects. For an interconnection structure, a standard double Au-layer interconnection was employed. The threshold voltage was optimized to approximately 0.0 V for high speed SCFL circuit operation. The transconductance was 530 mS/mm. The average cut-off frequency, f_T, and maximum frequency of oscillation, f_{max}, were 100 GHz and 101 GHz, respectively.

C. Measurement Set-up

The IC was tested on a wafer with dedicated 40 GHz bandwidth multiple contact probes. Figure 9 shows the measurement set-up. A complementary pair of the fundamental pseudo-random data stream (PN 2^7-1) up to 10 Gbit/s were generated from a pulse pattern generator (PPG). These were duplexed, delaying appropriately against each other by a GaAs MESFET MUX unit [10] to obtain a complementary data stream up to 20 Gbit/s. Furthermore, these were duplexed, also with appropriate delay against each other by a InP HFET MUX module [11], to obtain a data stream up to 40 Gbit/s, and then input to the decision IC. The output of the decision IC was demultiplexed to 20 Gbit/s by InP HFET demultiplexer module [11], and then to 10 Gbit/s by Si bipolar decision IC to confirm error-free operation using a 10 Gbit/s error detector (ED). The output of the decision IC was boosted by a commercial wide-band pulse amplifier to compensate for the input sensitivity of the InP demultiplexer module at 40 Gbit/s.

In the measurement set-up, the quality of the clock synchronization becomes more important as the data bit rate increases. A conventional 10 MHz synchronization between plural synthesized clock sources is insufficient for stable error-free confirmation and waveform observation. Therefore, 40 GHz clock signals for the decision IC and 10 GHz clock signals for MUX, DEMUX, PPG, and ED were generated from a single 20 GHz synthesized signal source (SG) using a doubler and a frequency divider, respectively.

D. Circuit Performance

The decision IC operated from under 20 Gbit/s to 40 Gbit/s. Figure 10 shows the input and

output eye diagrams at 40 Gbit/s. Good eye opening with a 1.1 Vp-p swing was obtained. It indicates that the output buffer satisfied the required bandwidth for 40 Gbit/s data signal. Figure 11 shows a 20 Gbit/s demultiplexed signal and a 10 Gbit/s demultiplexed signal in the 40 Gbit/s error-free confirmation. Under the above conditions, error-free operation at 40 Gbit/s was stably confirmed. The input sensitivity and phase margin of the IC at 40 Gbit/s was approximately 400 mV and one pico-second, respectively. A higher gain and wider bandwidth are required for the input buffers to improve the input sensitivity. The circuit speed reached 40% of the cut-off frequency of the FET. It is twice as high as a conventional master-slave static decision IC. This indicates that the super-dynamic flip-flop and wider bandwidth buffers are indispensable to the mitigation of the requirement for device speed performance.

CONCLUSION

We adopted wide-band amplifier circuits for clock and data buffers. This is the key to maximizing the decision circuit performance up to the FF speed limit. The super-dynamic decision IC fabricated with 0.15 µm gate length GaAs MESFETs successfully performed an error-free 40 Gbit/s operation. The FF speed approached 40 % of the cut-off frequency of the FET.

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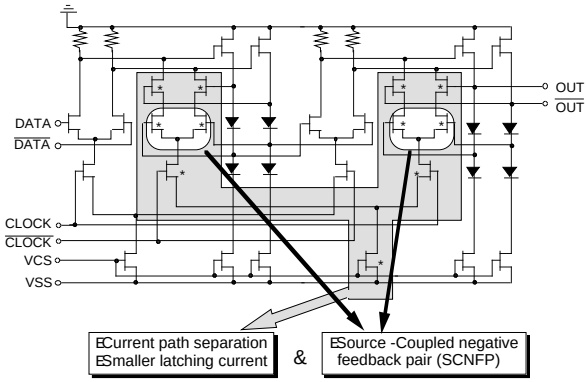


Fig. 1 Circuit diagram of the super-dynamic D-FF

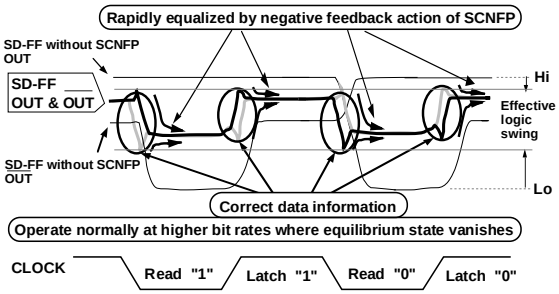


Fig. 2 Schematic output waveform of the super-dynamic D-FF at low clock frequency

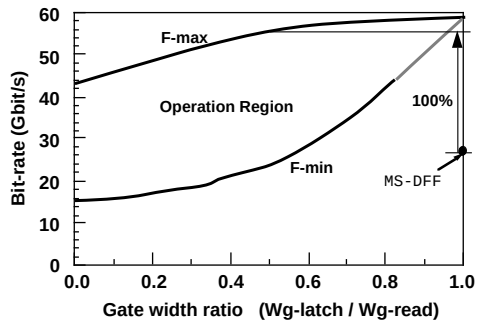


Fig. 3 The operation speed of the super-dynamic decision IC versus gate width ratio (Wg-latch/Wg-read)

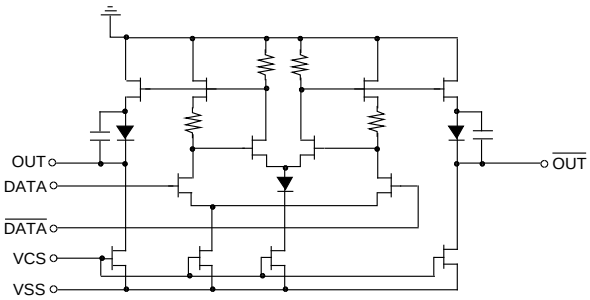


Fig. 4 Circuit diagram of the parallel feedback data buffer

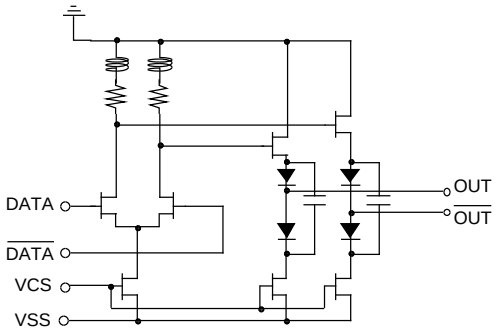


Fig. 5 Circuit diagram of the inductor-peaking output buffer

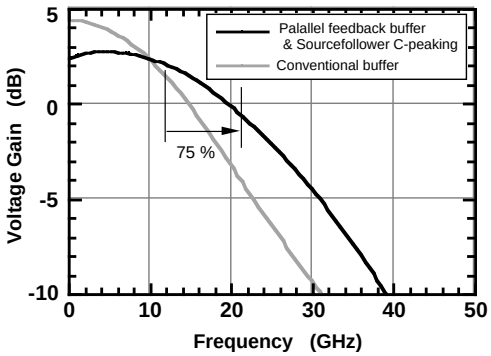


Fig. 6 Simulated gain-bandwidth of the parallel feedback input buffer

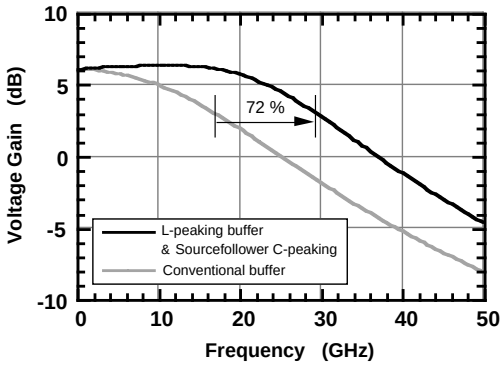


Fig. 7 Simulated gain-bandwidth of the inductor peaking output buffer

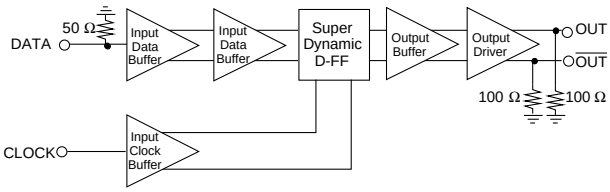


Fig. 8 Block diagram of the super-dynamic decision IC

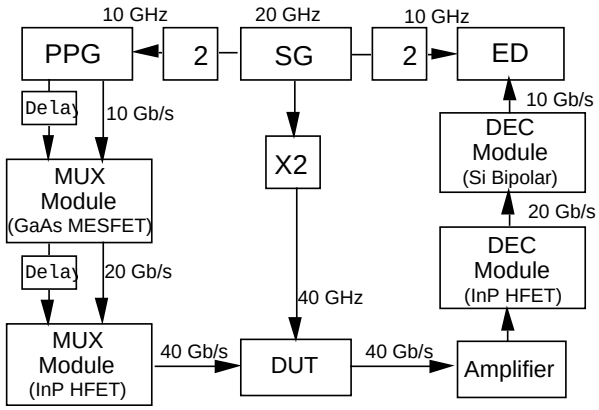
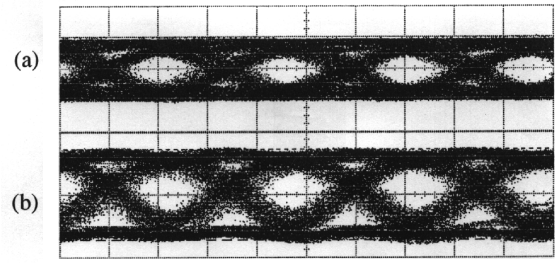
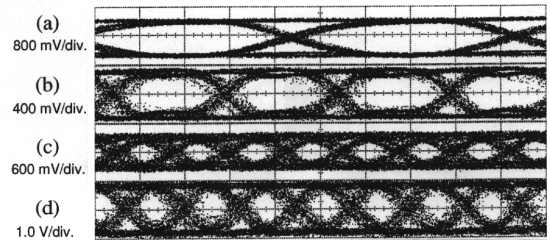


Fig. 9 Measurement Set-up



400 mV/div., 10 ps/div.

Fig. 10 Operating waveforms at 40Gbit/s
(a) Input
(b) Output



20 ps/div.

Fig. 11 Operating waveforms in 40Gbit/s error-free confirmation

(a) 10 Gbit/s demultiplexed signal (Si Bipolar DEC output)
(b) 20 Gbit/s demultiplexed signal (InP DEC output)
(c) 40 Gbit/s DUT input signal (InP MUX output)
(d) 40 Gbit/s output signal (Amplifier output)